

# LAKSHMI OMKARESWAR THUMMAGUNTA

+91-90002 45274 | [omkareswar.tl@gmail.com](mailto:omkareswar.tl@gmail.com) | [linkedin.com/in/omkar-tl](https://www.linkedin.com/in/omkar-tl) | [github.com/OmkarTL](https://github.com/OmkarTL)

## PROFESSIONAL SUMMARY

RTL Design and Verification enthusiast with hands-on experience in Verilog HDL-based digital design, simulation, and functional validation. Strong foundation in Computer Architecture, FPGA Design, and VLSI methodologies, with experience in developing and verifying processor, communication interface, and FSM-based digital designs.

## EDUCATION

|  |                                |
|--|--------------------------------|
| <b>B.E in Electronics and Communication Engineering, SCSVMV (Deemed to be University)</b><br>Honours in VLSI Design<br>CGPA – 8.74/10.00 | 2024 – 2027<br>Kanchipuram, TN |
| <b>Diploma in Electronics and Communication Engineering,</b><br><i>Audisankara College of Engineering &amp; Technology</i>               | 2021 – 2024<br>Nellore, AP     |

## TECHNICAL SKILLS

- Programming Languages:** Verilog HDL, SystemVerilog, VHDL, C-Programming, Python, Embedded C, MATLAB
- RTL & Digital Design:** RTL Design, FSM Design, Combinational Logic Design, Sequential Logic Design, Datapath Design, Computer Architecture, FPGA Design
- Design Verification:** Functional Verification, Testbench Development, Directed Testing, Simulation Debugging, Waveform Analysis
- Protocols & Interfaces:** UART, SPI, I2C, GPIO
- Embedded Systems:** ESP32, 8051 Microcontroller, Hardware Interfacing, Sensor Integration
- EDA & Development Tools:** Xilinx Vivado, ModelSim, GTKWave, LTspice, PSpice, Multisim, MATLAB, Code Composer Studio, IAR Embedded Workbench, VS Code, Arduino IDE, Cisco Packet Tracer
- Domains:** RTL Design, Design Verification, FPGA Design, VLSI Design, Embedded Systems

## EXPERIENCE

|  |   |
|--|---|
| <b>Internship Trainee, Andhra Pradesh Power Generation Corporation Limited</b><br>Studied real-time operations of an 800 MW power generation unit, including turbine and electrical distribution systems, supported efficiency analysis and daily performance data logging, contributing to maintenance decisions<br>Collaborated with industry professionals to strengthen problem-solving abilities and gain practical exposure to power systems, energy management, and technical analysis. | 11/2023 – 05/2024<br>Nellore, Andhra Pradesh, India |
|--|---|

## PROJECTS

### 8-Bit Single-Cycle RISC Processor | Verilog HDL | [GitHub Link](#)

Designed and verified an 8-bit single-cycle RISC processor featuring ALU, Register File, Control Unit, Program Counter, and Memory Interface modules. Performed functional verification using custom testbenches and waveform analysis to validate instruction execution and Datapath operations.

### UART Transmitter | Verilog HDL | [GitHub Link](#)

Implemented an FSM-based UART transmitter with configurable baud-rate generation for asynchronous serial communication. Developed verification testbenches to validate protocol compliance, timing accuracy, and reliable data transmission under multiple scenarios.

### Traffic Light Controller | Verilog HDL | [GitHub Link](#)

Performed functional verification of an FSM-based traffic light controller by validating state transitions, timing constraints, and output responses. Created simulation scenarios, analyzed waveforms, and identified design issues to ensure compliance with operational specifications.

## CERTIFICATIONS & RECOGNITIONS

**CAMPUS AMBASSADOR – PALS - IIT Alumni initiative** **2024 - Present**

### VLSI Design – Internshala

- Covered core HDL fundamentals, combinational & sequential logic, FSMs, and FPGA system design

### Computer Networks and Internet Protocol – NPTEL

- Covered core networking concepts including the OSI/TCP-IP models, routing protocols, and internet communication standards.

**Finalist, InnoWAH Challenge (PALS)** – Recognized for designing a smart, sensor-driven automated system with real-world impact.